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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MENZ, DOUGLAS M	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/660,677	NAKAJIMA ET AL.	
	Examiner	Art Unit	
	Douglas M. Menz	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/11/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: Search History.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10, 13, 16 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhattacharyya et al. (US 6597049).

Regarding claim 1, Bhattacharyya discloses a magnetic memory device comprising:

first wirings (24, Fig. 9a) which run in a first direction and are divided in a second direction different from the first direction;

a second wiring (22, Fig. 9a) which runs in the second direction; and

a first magneto-resistive element (20) which is arranged across the first divided wirings near an intersection of the first and second wirings in a first memory cell region.

Regarding claim 2, Bhattacharyya further discloses wherein the first wirings (24) are divided on the same plane (Figs. 9a-b).

Regarding claim 3, Bhattacharyya further discloses wherein a distance between the first wirings (S_2) is shorter than a length of the first magneto-resistive element (L) in the second direction (Fig. 9b).

Regarding claim 4, Bhattacharyya further discloses wherein an intensity of a magnetic field generated upon supplying a current to the wirings has a plurality of maximum values (*i.e. concentrated field*) within a plane of the first magneto-resistive element (Col. 11, lines: 10-15).

Regarding claim 5, Bhattacharyya further discloses wherein the maximum value exists at an end of the first magneto-resistive element (Col. 11, lines: 10-15).

Regarding claim 6, Bhattacharyya further discloses wherein the second wiring (22) is divided into a plurality of wirings in the first direction (Fig. 9a).

Regarding claim 7, Bhattacharyya further discloses wherein a distance between the second divided wirings (S_1) is shorter than a length of the first magneto-resistive element (W) in the first direction (Fig. 8b).

Regarding claims 8-9, Bhattacharyya further discloses wherein the first wirings include word lines or bit lines (The conductors of Bhattacharyya correspond to word

lines or bit lines of an MRAM structure as disclosed in the background of the art in Col. 1, lines: 63-67 and Col. 2, lines: 15-27, which correspond to Figs. 2-3. The names "bit lines" and "word lines" are for nomenclature purposes only, either the top conductors or the bottom conductors can be either one.

Regarding claim 10, Bhattacharyya further discloses wherein, of the first divided wirings (24), one wiring is arranged in contact with the first magneto-resistive element, and the other wiring is arranged apart from the first magneto-resistive element (Fig. 9c and Col. 6, lines: 27-31 and Col. 10, lines: 35-40).

Regarding claim 13, Bhattacharyya further discloses a second memory cell region adjacent to one side of the first memory cell region (*20, first row second column of Fig. 9a*),

A third memory cell region adjacent to the other side of the first memory cell region (*20, second row first column of Fig. 9a*),

A second magneto-resistive element which is arranged in the second memory cell region (*20, first row second column of Fig. 9a*), and

A third magneto-resistive element which is arranged in the third memory cell region (*20, second row first column of Fig. 9a*), and

In which said one wiring 24 runs from the first memory cell region into the second memory cell region (Fig. 9a), and

Said other wiring 22 runs from the first memory cell region into the third memory cell region (Fig. 9a), and

The wirings (*i.e. conductors*) can be arranged apart from or in contact with the magneto-resistive elements (Col. 6, lines: 27-31).

Regarding claim 16, Bhattacharyya further discloses wherein the first divided wirings (24, Fig. 9a) are connected in a peripheral circuit region outside the first memory cell region (20, Fig. 9a and Col. 10, lines: 47-60).

Regarding claim 18, Bhattacharyya further discloses a fourth memory cell (*20, second column first row counting left to right top to bottom, Fig. 9a*) adjacent to the first memory cell (*20, first column first row, Fig. 9a*) region in the first direction, which has a magneto-resistive element (20, Fig. 9a), and

In which one of the first divided wirings is used as a write wiring of the fourth magneto-resistive element (*Bhattacharyya's conductor structure requires a current through both the x axis and the y axis as disclosed in Col. 3. Therefore, one can conclude that one of the first divided wirings is used as a write wiring of the fourth magneto-resistive element*).

Regarding claim 19, Bhattacharyya further discloses wherein a width of each of the first wirings (24, Fig. 9b) is shorter than a length (L, Fig. 9) of the first magneto-resistive element in the second direction.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya et al. (US 6597049) in view of Deak (US 6728132).

Bhattacharyya discloses the structure of claims 10, 13 as mentioned above. Bhattacharyya further discloses wherein both conductors are required to write to a

magneto-resistive element (Col. 2, lines: 1-12). However, Bhattacharyya does not explicitly disclose wherein one of the conductors is used as a write/read conductor.

Deak discloses the operation of a typical MRAM device which has 2 orthogonal conductors for which both are used for writing and only one is used to read the data (Cols. 1-2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have Bhattacharyya's 2 orthogonal conductors for which both are used for writing and only one is used to read the data since this is a commonly known mode of operation as taught by Deak (Cols. 1-2).

Claims 12 and 15 are rejected under 35 U.S.C. 103(a) as being obvious over Bhattacharyya et al. (US 6597049) in view of Nakajima et al. (US 6473336).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer

in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Bhattacharyya discloses the structure of claims 10 and 13 as mentioned above. However, Bhattacharyya does not disclose wherein the magneto-resistive elements have a step. Nakajima discloses a magnetic memory device, which incorporates a magneto-resistive element with a step (111, Fig. 19 and Col. 21, lines: 20-25).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include a magneto-resistive element with a step into Bhattacharyya's conductor structure because Bhattacharyya's structure pertains to the conductors used in magnetic memory devices in general. Bhattacharyya further discloses that various memory cell arrangements can be incorporated into the conductor structure (Col. 6, lines: 19-30) and a magneto-resistive element with a step was known at the time of the invention.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya et al. (US 6597049) in view of Arai et al. (US 6538946).

Bhattacharyya discloses the structure of claim 16 as mentioned above. However, Bhattacharyya does not explicitly disclose wherein the pitch between the wirings of the memory cell area are different than a pitch of the wirings in the peripheral

circuit region. Arai discloses a memory structure which has memory cell regions and peripheral regions wherein the pitch of the corresponding bitlines is different (Fig. 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have different wiring pitches between the memory cell wirings and the peripheral wirings as taught by Arai because of the dynamics of scale between the memory cells and the peripheral circuitry associated with memory arrays such as sensing circuitry.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas M. Menz whose telephone number is 571-272-1877. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DM Doug Menz 6/23/05